Design of Analog CMOS Integrated Circuits

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Errata in Problem Sets

Chapter 2

- In Eq. (2.44), μ_n must be in the numerator.

Chapter 3

- Call the third problem 3.2'.
- In Problem 3.2, Fig. 3.68(d), change the gate voltage of M_2 to V_{b2}.
- In Problem 3.4, Fig. 3.71(a), change the gate voltage of $M_=1$ to V_{b1}.
- In Fig. 3.72(e), V_{b1} must be changed to V_{in}.
- In Fig. 3.73(h), the output is at the source of M_2.
- In Problem 3.10(c), the question must be phrased as: Which device enters the triode region first as V_{out} falls?
- In Problem 3.13, first sentence should read: ... with $W/L = 50/0.5$ ...
- In Problem 3.16(a), do not neglect channel-length modulation in the triode region.

Chapter 4

- In Problem 4.2, assume $I_{SS} = 1$ mA and change part (a) to: Determine the voltage gain.
- In Problem 4.6, assume $\lambda = 0$.
- In Problem 4.9, assume $\lambda = \gamma = 0$.
- In Problem 4.11, assume $I_{D5} = 20$ μA.
- In Problem 4.13, change the figure number to 4.8(a).

Chapter 5

- In Problem 5.16(d), assume V_{TH} does not vary with temperature.

Chapter 6

- In Problem 6.4(b) and (d), assume $\lambda \neq 0$.

Chapter 7

- The second sentence of Problem 7.2 should read: Assume $(W/L)_1 = 50/0.5, I_{D1} = I_{D2} = 0.1$ mA ...
- In Problem 7.20, change I_{D1} and I_{D2} to 0.05 mA.
- In Problem 7.24, change the bias current to 0.1 mA.

Chapter 8

- In Problem 8.10, change the tolerable gain error to 5%.
- In Problem 8.15, Fig. 8.55(b), call label the top G_m block G_{m2}. The output is at the output nodes of G_{m2}.

Chapter 10

- In Problem 10.11, change I_{SS} to 0.25 mA and $(W/L)_{5,6}$ to 60/0.5.
- In Problem 10.12, add: Maximize $V_{GS14} = V_{GS15}$ while leaving at least 0.5 V across I_1. Also, in part (b), change M_2 to M_1.
- Problem 10.17 should read: ... between the gate and the drain of M_2 or M_3.
- In Fig. 10.42, change the gate voltage of $M_{3,4}$ to V_{b1}.
- In Problem 10.19(c), change A_0 in the numerator to A.

Chapter 11

- In Problem 11.13, ... such that the circuit operates with $V_{DD} = 3$ V.
- In Problems 11.17 and 11.18, the top terminal of R_2 should be connected to the top terminal of R_1.
- In Problem 11.22, assume $K = 4$.

Chapter 12

- In Problem 12.8, assume $C_H = 1$ pF.
- In Problem 12.12, assume all switches are NMOS devices.
- In Problem 12.14, assume $C_{in} = 0.2$ pF and calculate C_1 and C_2.
- In Problem 12.16, the output is sensed at the drains of M_1 and M_2.

Chapter 13

- In Problem 13.5, change the figure number to 13.6(a).